Memory Interface of 8086/8088 Microprocessors

This presentation will explore the memory interface of the 8086/8088 microprocessors, focusing on memory organization, addressing modes, and the key signals involved in memory access.

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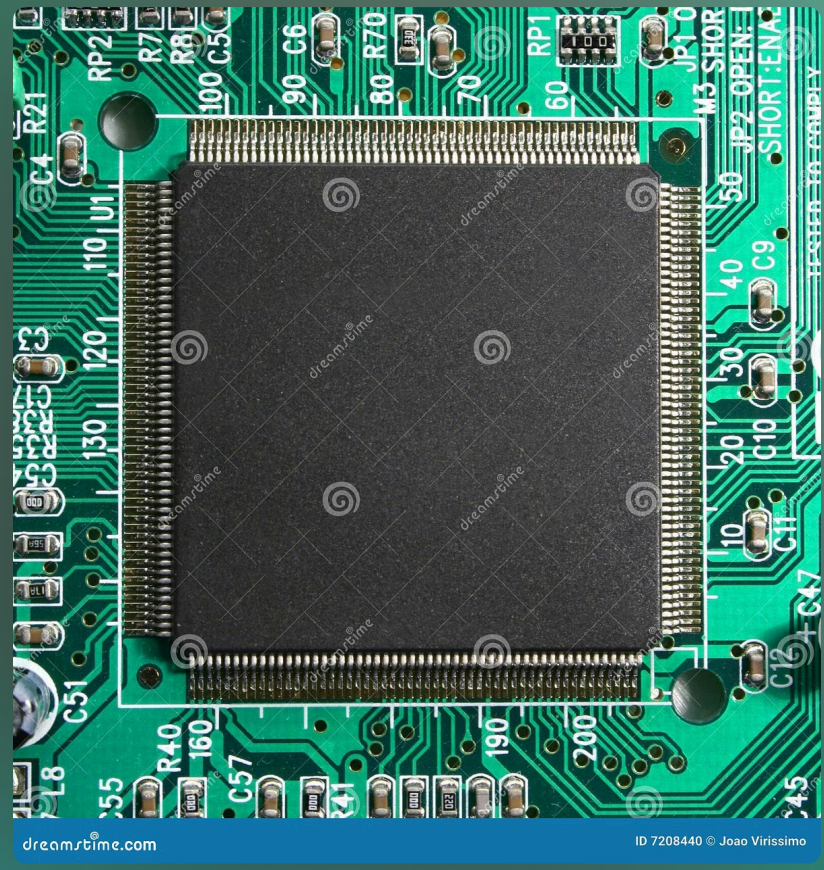


Memory Organization in 8086/8088

Segmented Architecture

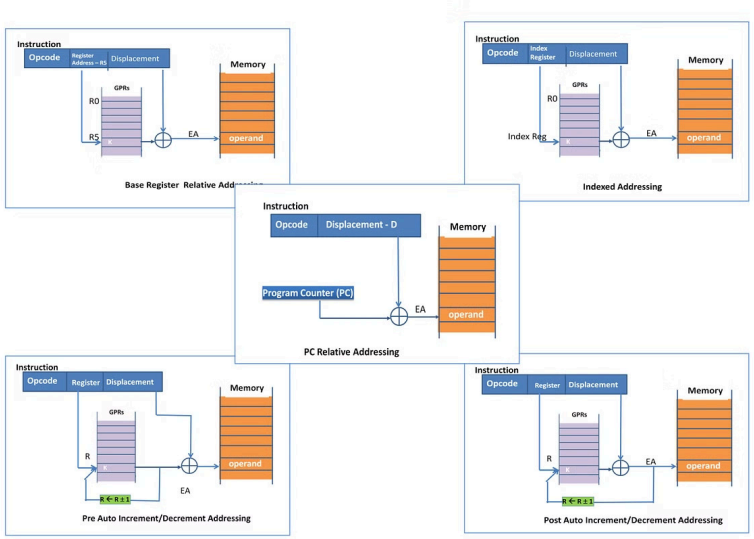
The 8086/8088 employs a segmented memory architecture, where memory is divided into 64KB segments.

Logical Address

The CPU generates a logical address consisting of a segment selector and an offset within the segment.

Physical Address

The memory management unit (MMU) translates the logical address into a physical address, which is the actual address used by the memory controller.



Memory Addressing Modes

1 **Register Addressing**

The operand is located at the address stored in a register.

2 **Immediate Addressing**

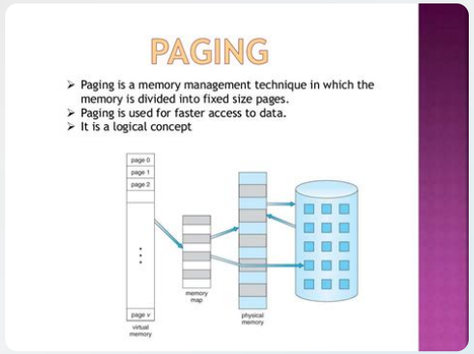
The operand is directly included in the instruction.

3 **Direct Addressing**

The operand's address is explicitly specified in the instruction.

4 **Indirect Addressing**

The operand's address is stored in a memory location, and the instruction specifies the address of this location.



Memory Segmentation and Paging

Segmentation

Memory is divided into 64KB segments, allowing for more efficient memory management and protection.

1

Paging

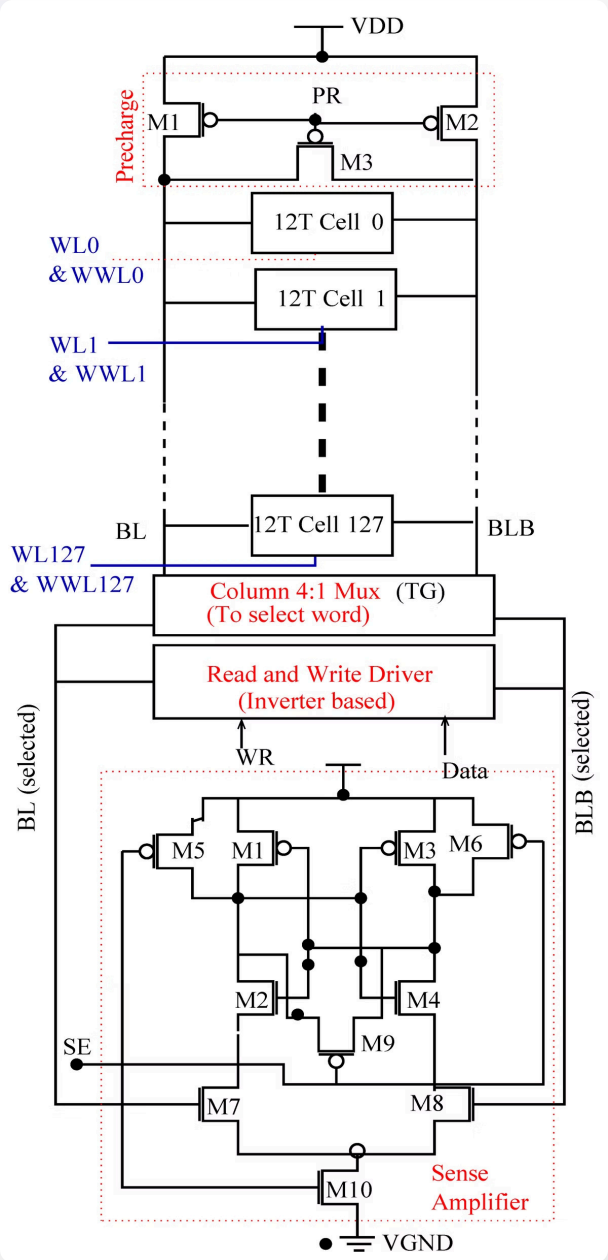
The 8086/8088 does not implement paging. Paging is a feature of later processors, like the 80386, that allows for finer-grained memory management.

2

Combined Approach

Segmentation provides logical memory organization, while paging offers finer-grained control, creating a robust memory architecture.

3



Memory Read and Write Operations

1

Read Operation

The CPU sends the address of the memory location to be read to the memory controller.

2

Data Transfer

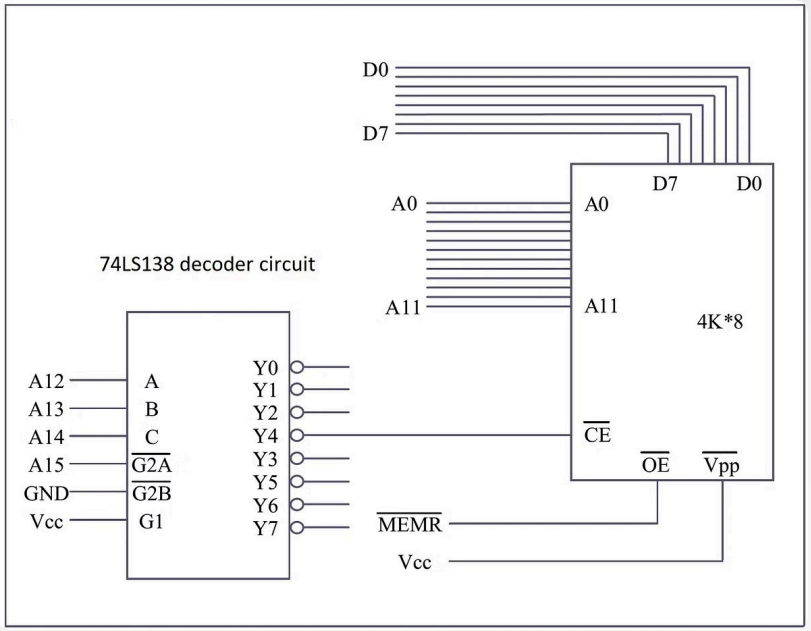
The memory controller fetches the data from the specified memory location and sends it to the CPU.

3

Write Operation

The CPU sends the data to be written to the memory controller along with the address of the destination location.

Memory Interface Signals



Signal	Description
Address Bus (A0-A19)	Carries the physical address of the memory location to be accessed.
Data Bus (D0-D15)	Transmits data between the CPU and memory.
Read/Write (RD/WR)	Indicates whether the operation is a read or a write.
Memory Request (MEMR)	Signals the memory controller that the CPU is requesting a memory operation.
Memory Acknowledge (MEMW)	Indicates that the memory controller has received the memory request.

Memory Timing and Protocols

Clock Cycles

The timing of memory operations is synchronized with the CPU clock cycle.

Bus Cycles

A memory operation consists of several bus cycles, each involving data transfer and control signals.

Memory Protocols

Different memory technologies use different protocols, defining the timing and sequence of signals during memory access.

Memory Latency

The time delay between a memory request and the completion of the operation is called memory latency.

Conclusion and Key Takeaways

Memory Organization

The 8086/8088 uses a segmented memory architecture with logical and physical addresses.

Addressing Modes

Different addressing modes provide flexibility in accessing data within memory.

Memory Interface Signals

Control signals manage the flow of data and communication between the CPU and memory.

Timing and Protocols

Memory operations are synchronized with the CPU clock cycle and follow specific protocols for data transfer.